Artix-7 FPGAs Data Sheet: DC and Switching Characteristics

DS181 (v1.1) November 7, 2011 **Advance Product Specification**

Artix-7 FPGA Electrical Characteristics

Artix™-7 FPGAs are available in -3, -2, -1, and -2L speed grades, with -3 having the highest performance. The -2L devices can operate at either of two voltages, 0.9V and 1.0V and are screened for lower maximum static power. When operated at 1.0V, the speed specification of a -2L device is the same as the -2 speed grade. When operated at 0.9V, the -2L static and dynamic power is reduced and the performance is similar to a -1 device.

Artix-7 FPGA DC and AC characteristics are specified in commercial, extended, and industrial temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Artix-7 FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/7.

All specifications are subject to change without notice.

Artix-7 FPGA DC Characteristics

Table 1: **Absolute Maximum Ratings (1)**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 2.0	V
V_{CCO}	Output drivers supply voltage relative to GND for 3.3V HR I/O banks	–0.5 to 3.6	V
V_{CCBRAM}	Supply voltage for the block RAM memories	–0.5 to 1.1	V
V_{CCADC}	XADC supply relative to GNDADC	–0.5 to 2.0	V
V_{CCBATT}	Key memory battery backup supply	–0.5 to 2.0	V
V_{REF}	Input reference voltage	–0.5 to 2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5 to 2.0	V
V_{IN}(2)	I/O input voltage relative to GND(3) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 3.3V or below output(3) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(4)	+220	°C
T_j	Maximum junction temperature(4)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The 3.3V I/O absolute maximum limit applied to DC and AC signals.
3. For I/O operation, refer to UG471: *7 Series FPGAs SelectIO Resources User Guide*.
4. For soldering guidelines and thermal considerations, see UG475: *7 Series FPGA Packaging and Pinout Specification*.

Table 2: **Recommended Operating Conditions (1)**

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_j = 0°C to +85°C	0.95	1.05	V
	For -2L (0.9V) devices: internal supply voltage relative to GND, T_j = 0°C to +85°C	0.87	0.93	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_j = 0°C to +85°C	1.71	1.89	V
V_{CCO}(2)(4)	Supply voltage for 3.3V HR I/O banks relative to GND, T_j = 0°C to +85°C	1.14	3.47	V
V_{CCBRAM}	Block RAM supply voltage	0.95	1.05	V
V_{CCBATT}(3)	Battery voltage relative to GND, T_j = 0°C to +85°C	1.0	1.89	V
V_{IN}	I/O input voltage relative to GND, T_j = 0°C to +85°C	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}(5)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA

Notes:

1. All voltages are relative to ground.
2. Configuration data is retained even if V_{CCO} drops to 0V.
3. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. A total of 100 mA per bank should not be exceeded.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)				V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)				V
I_{REF}	V_{REF} leakage current per pin				µA
I_L	Input or output leakage current per pin (sample-tested)				µA
C_{IN}(2)	Die input capacitance at the pad				pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V				µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V				µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V				µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V				µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V				µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V				µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V				µA
I_{BATT}(3)	Battery supply current				nA
n	Temperature diode ideality factor		1.0002		–
r	Series resistance		2		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.

Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at T_j = 85°C because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Artix-7 devices. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7A8					mA
		XC7A15					mA
		XC7A30T					mA
		XC7A50T					mA
		XC7A100T					mA
		XC7A200T					mA
		XC7A350T					mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7A8					mA
		XC7A15					mA
		XC7A30T					mA
		XC7A50T					mA
		XC7A100T					mA
		XC7A200T					mA
		XC7A350T					mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7A8					mA
		XC7A15					mA
		XC7A30T					mA
		XC7A50T					mA
		XC7A100T					mA
		XC7A200T					mA
		XC7A350T					mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7A8					mA
		XC7A15					mA
		XC7A30T					mA
		XC7A50T					mA
		XC7A100T					mA
		XC7A200T					mA
		XC7A350T					mA

Notes:
1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j).
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

There are no sequencing requirements for the GTP transceiver supplies with respect to the other FPGA supply voltages.

Table 5 shows the minimum current, in addition to I_{CCQ}, that are required by Artix-7 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 5: **Power-On Current for Artix-7 Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	I_{CCBRAM}	Units
	Typ(1)	Typ(1)	Typ(1)	Typ(1)	
XC7A8					mA
XC7A15					mA
XC7A30T					mA
XC7A50T					mA
XC7A100T					mA
XC7A200T					mA
XC7A350T					mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100°C$(1)	–	500	ms
		$T_J = 85°C$(1)	–	800	

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: **SelectIO DC Input and Output Levels** (1)

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.3	0.8	2.0	3.45	0.4	2.4	Note 2	Note 2
LVCMOS33	–0.3	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	Note 3	Note 3
LVCMOS25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note 3	Note 3
LVCMOS18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note 2	Note 2
LVCMOS15	–0.3	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note 4	Note 4
PCI33_3	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
HSTL I(5)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(5)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
DIFF HSTL I(5)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(5)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL135	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3				
DIFF SSTL135	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3				
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	8	–8
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.608	V_{TT} + 0.608	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
SSTL15	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	V_{TT} – 0.175	V_{TT} + 0.175	17.8	17.8

Notes:

1. Tested according to relevant specifications.
2. Supported drive strengths of 4, 8, 12, 16, or 24 mA.
3. Supported drive strengths of 4, 8, 12, or 16 mA.
4. Supported drive strengths of 4, 8, or 12 mA.
5. Applies to both 1.5V and 1.8V HSTL.
6. For detailed interface specific DC voltage levels, see UG471: *7 Series FPGAs SelectIO Resources User Guide*.

LVDS DC Specifications (LVDS_25)

See UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information on the LVDS_25 standard in the HR I/O banks.

Table 8: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.00	1.25	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	1.425	V

eFUSE Read Endurance and Programming Conditions

Table 9 lists the maximum number of read cycle operations expected. Table 10 lists the programming conditions specifically for eFUSE. For more information, see UG470: *7 Series FPGA Configuration User Guide*.

Table 9: **eFUSE Read Endurance(1)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.					Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.					Read Cycles

Notes:

1. Power-up cycles must be added when counting the number of read cycles.

Table 10: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

GTP Transceiver Specifications

GTP Transceiver DC Characteristics

Table 11: **Absolute Maximum Ratings for GTP Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTP transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.26	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 12: **Recommended Operating Conditions for GTP Transceivers (1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	0.97	1.0	1.03	V
MGTAVTT	Analog supply voltage for the GTP transmitter and receiver termination circuits relative to GND	1.17	1.2	1.23	V

Notes:

1. Each voltage listed requires the filter circuit described in UG476: *7 Series FPGAs Transceiver User Guide*.
2. Voltages are specified for the temperature range of T_j = 0°C to +85°C.

Table 13: **GTP Transceiver Current Supply**

Symbol	Description	Typ(1)	Max	Units
$I_{MGTAVCC}$	MGTAVCC supply current for one GTP Quad (4 lanes)		Note 2	mA
$I_{MGTAVTT}$	MGTAVTT supply current for one GTP Quad (4 lanes)			mA

Notes:

1. Typical values are specified at nominal voltage, 25°C, at the maximum line rate.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 14: **GTP Transceiver Quiescent Supply Current(1)(2)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current for one GTP Quad (4 lanes)		Note 3	mA
$I_{MGTAVTTQ}$	Quiescent MGTAVTT supply current for one GTP Quad (4 lanes)			mA

Notes:

1. Device powered and unconfigured.
2. GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.
3. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
4. Typical values are specified at nominal voltage, 25°C.

GTP Transceiver DC Input and Output Levels

Table 15 summarizes the DC output specifications of the GTP transceivers in Artix-7 FPGAs. Consult UG476: *7 Series FPGAs Transceiver User Guide* for further details.

Table 15: **GTP Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled		–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTT = 1.2V	–400	–	MGTAVTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTT = 1.2V	–	2/3 MGTAVTT	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage	Equation based	MGTAVTT – DV_{PPOUT}/4			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled		1/2 MGTAVTT			mV
R_{IN}	Differential input resistance			100		Ω
R_{OUT}	Differential output resistance			100		Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (Flip-chip packages)		–	–	10	ps
	Transmitter output pair (TXP and TXN) intra-pair skew (Wire-bond packages)		–	–	12	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG476: *7 Series FPGAs Transceiver User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

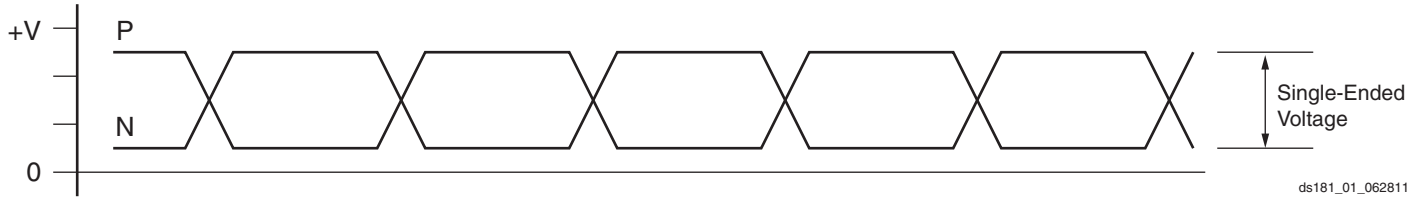

Figure 1: **Single-Ended Peak-to-Peak Voltage**

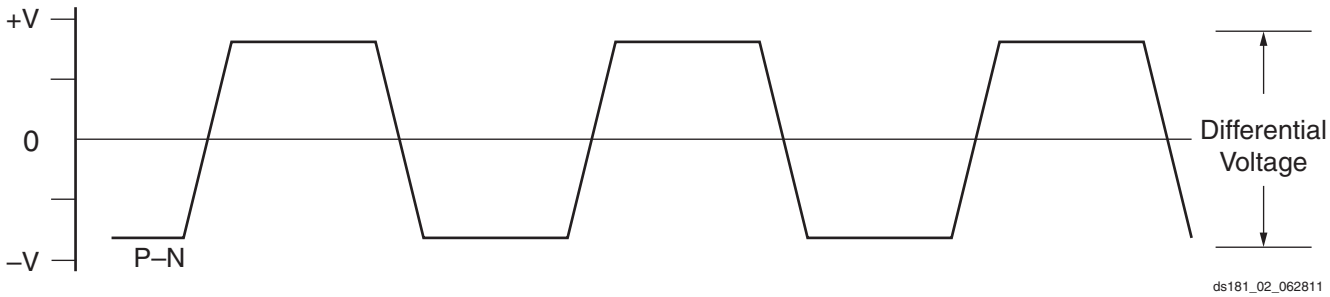

Figure 2: **Differential Peak-to-Peak Voltage**

Table 16 summarizes the DC specifications of the clock input of the GTP transceiver. Consult UG476: *7 Series FPGAs Transceiver User Guide* for further details.

Table 16: **GTP Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250		2000	mV
R_{IN}	Differential input resistance		100		Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult UG476: *7 Series FPGAs Transceiver User Guide* for further information.

Table 17: **GTP Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade				Units
			1.0V			0.9V	
			-3(1)	-2/-2L(1)	-1	-2L	
F_{GTPMAX}	Maximum GTP transceiver data rate		6.6	6.6	3.75	3.75	Gb/s
F_{GTPMIN}	Minimum GTP transceiver data rate		0.500	0.500	0.500	0.500	Gb/s
$F_{GTPRANGE}$	PLL line rate range	1	3.2–6.6	3.2–6.6	3.2–3.75	3.2–3.75	Gb/s
		2	1.6–3.3	1.6–3.3	1.6–3.2	1.6–3.2	Gb/s
		4	0.8–1.65	0.8–1.65	0.8–1.6	0.8–1.6	Gb/s
		8	0.5–0.825	0.5–0.825	0.5–0.8	0.5–0.8	Gb/s
$F_{GTPPLLRANGE}$	GTP transceiver PLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	1.6–3.3	GHz

Notes:

1. F_{GTPMAX} is limited to 5.4 Gb/s in wire bond packages.

Table 18: **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$F_{GTPDRPCLK}$	GTPDRPCLK maximum frequency	156	156	125	125	MHz

Table 19: **GTP Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{TXOUT}	TXUSERCLKOUT maximum frequency		60	–	660	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	–	60	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–		ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–		µs

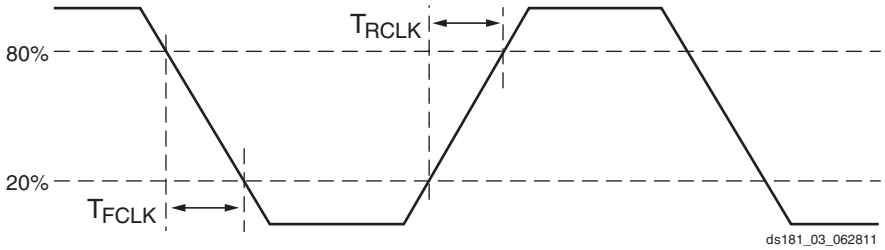

Figure 3: **Reference Clock Timing Parameters**

Table 20: **GTP Transceiver User Clock Switching Characteristics** (1)

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
F_{TXOUT}	TXOUTCLK maximum frequency		412.5	412.5	234.375	234.375	MHz
F_{RXOUT}	RXOUTCLKT maximum frequency		412.5	412.5	234.375	234.375	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.5	412.5	234.375	234.375	MHz
		32-bit data path	206.25	206.25	117.1875	117.1875	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.5	412.5	234.375	234.375	MHz
		32-bit data path	206.25	206.25	117.1875	117.1875	MHz

Notes:

1. Clocking must be implemented as described in UG476: *7 Series FPGAs Transceiver User Guide*.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 21: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$F_{PIPECLK}$	Pipe clock maximum frequency	250	250	250	250	MHz
$F_{USERCLK}$	User clock maximum frequency	250	250	250	250	MHz
$F_{USERCLK2}$	User clock 2 maximum frequency	250	250	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

XADC Specifications

Table 22: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, T_j = –40°C to 100°C, Typical values at T_j=+40°C						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral Nonlinearity	INL		–	–	±2	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Calibrated	–	–	±4	LSBs
Gain Error		Calibrated	–	–	±0.4	%
Channel Matching		Based on two individual ADC instances with calibration enabled	–	–	10	LSBs
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio	SNR	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion	THD	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	75	–	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs(2)						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz

Table 22: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
On-Chip Sensors						
Temperature Sensor Error		T_j = –40°C to 100°C.	–	–	±4	°C
		T_j = –55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –40°C to +100°C	–	–	±1	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –55°C to +125°C	–	–	±2	%
Conversion Rate(3)						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%
XADC Reference(4)						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
Power Requirements						
Analog Power Supply	V_{CCADC}		1.71	1.8	1.89	V
Analog Supply Current	I_{CCADC}	Analog circuits in powered up state	–	–	20	mA

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature.
2. See the ADC chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
3. See the Timing chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
4. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 14.

Table 23: **Networking Applications Interface Performances**

Description	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)					Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 10)					Mb/s
SDR LVDS receiver (SFI-4.1)(1)					Mb/s
DDR LVDS receiver (SPI-4.2)(1)					Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 24: **Maximum Physical Interface (PHY) Rate for Memory Interfaces (1)**

Memory Standard	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
DDR3	1066	800	800		Mb/s
DDR3L	800	800	667		Mb/s
DDR2	800	800	667		Mb/s
LPDDR2	667	667	533		Mb/s

Notes:

1. Advance performance numbers pending characterization on Xilinx memory platforms designed according to the guidelines in the *7 Series FPGAs Memory Interface Solutions User Guide*.

Switching Characteristics

All values represented in this data sheet are based on the advance speed specifications in ISE® software 13.3 v1.02 for the -3, -2, and -1 speed grades.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 25 correlates the current status of each Artix-7 device on a per speed grade basis.

Table 25: **Artix-7 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7A8	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7A15	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7A30T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7A50T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7A100T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7A200T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7A350T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Artix-7 devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 26 lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 26: **Artix-7 Device Production Software and Speed Specification Release**

Device	Speed Grade			
	1.0V			0.9V
	-3	-2/-2L	-1	-2L
XC7A8				
XC7A15				
XC7A30T				
XC7A50T				
XC7A100T				
XC7A200T				
XC7A350T				

Notes:
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

IOB Pad Input/Output/3-State Switching Characteristics

Table 27 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 28 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 27: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTL_S4	1.58	1.72	1.93		5.85	6.33	7.06		5.85	6.33	7.06		ns
LVTTL_S8	1.58	1.72	1.93		5.85	6.33	7.06		5.85	6.33	7.06		ns
LVTTL_S12	1.58	1.72	1.93		4.68	4.92	5.29		4.68	4.92	5.29		ns
LVTTL_S16	1.58	1.72	1.93		4.65	4.90	5.27		4.65	4.90	5.27		ns
LVTTL_S24	1.58	1.72	1.93		3.64	4.08	4.72		3.64	4.08	4.72		ns
LVTTL_F4	1.58	1.72	1.93		5.86	6.28	6.89		5.86	6.28	6.89		ns
LVTTL_F8	1.58	1.72	1.93		5.75	6.20	6.89		5.75	6.20	6.89		ns
LVTTL_F12	1.58	1.72	1.93		4.56	4.80	5.15		4.56	4.80	5.15		ns
LVTTL_F16	1.58	1.72	1.93		4.56	4.79	5.14		4.56	4.79	5.14		ns
LVTTL_F24	1.58	1.72	1.93		2.66	3.44	4.60		2.66	3.44	4.60		ns
LVDS_25	0.72	0.78	0.87		1.41	1.50	1.65		1.41	1.50	1.65		ns
MINI_LVDS_25	0.71	0.77	0.85		1.41	1.50	1.65		1.41	1.50	1.65		ns
BLVDS_25	0.72	0.79	0.89		1.93	2.13	2.41		1.93	2.13	2.41		ns
RSDS_25 (point to point)	0.71	0.78	0.88		1.41	1.50	1.65		1.41	1.50	1.65		ns
PPDS_25	0.74	0.80	0.90		1.38	1.50	1.68		1.38	1.50	1.68		ns
TMDS_33	0.85	0.93	1.06		1.47	1.57	1.71		1.47	1.57	1.71		ns
PCI33_3	1.55	1.69	1.91		2.97	3.28	3.75		2.97	3.28	3.75		ns
HSUL_12	0.66	0.70	0.76		2.34	2.66	3.14		2.34	2.66	3.14		ns
DIFF_HSUL_12	0.63	0.68	0.76		1.96	2.19	2.54		1.96	2.19	2.54		ns
HSTL_I_S	0.67	0.72	0.79		1.54	1.67	1.86		1.54	1.67	1.86		ns
HSTL_II_S	0.67	0.72	0.79		1.14	1.22	1.34		1.14	1.22	1.34		ns
HSTL_I_18_S	0.68	0.72	0.79		1.32	1.43	1.59		1.32	1.43	1.59		ns
HSTL_II_18_S	0.68	0.72	0.79		1.20	1.29	1.42		1.20	1.29	1.42		ns
DIFF_HSTL_I_S	0.72	0.76	0.83		1.43	1.54	1.71		1.43	1.54	1.71		ns
DIFF_HSTL_II_S	0.72	0.76	0.83		1.10	1.18	1.29		1.10	1.18	1.29		ns
DIFF_HSTL_I_18_S	0.73	0.78	0.86		1.26	1.35	1.50		1.26	1.35	1.50		ns

Table 27: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_18_S	0.73	0.78	0.86		1.10	1.18	1.29		1.10	1.18	1.29		ns
HSTL_I_F	0.67	0.72	0.79		1.10	1.19	1.33		1.10	1.19	1.33		ns
HSTL_II_F	0.67	0.72	0.79		0.99	1.08	1.21		0.99	1.08	1.21		ns
HSTL_I_18_F	0.68	0.72	0.79		1.07	1.16	1.30		1.07	1.16	1.30		ns
HSTL_II_18_F	0.68	0.72	0.79		1.00	1.09	1.22		1.00	1.09	1.22		ns
DIFF_HSTL_I_F	0.72	0.76	0.83		1.04	1.13	1.26		1.04	1.13	1.26		ns
DIFF_HSTL_II_F	0.72	0.76	0.83		0.97	1.05	1.17		0.97	1.05	1.17		ns
DIFF_HSTL_I_18_F	0.73	0.78	0.86		1.03	1.12	1.24		1.03	1.12	1.24		ns
DIFF_HSTL_II_18_F	0.73	0.78	0.86		0.96	1.04	1.16		0.96	1.04	1.16		ns
LVCMOS33_S4	1.79	1.91	2.10		5.68	6.09	6.70		5.68	6.09	6.70		ns
LVCMOS33_S8	1.79	1.91	2.10		4.82	5.27	5.95		4.82	5.27	5.95		ns
LVCMOS33_S12	1.79	1.91	2.10		3.88	4.29	4.90		3.88	4.29	4.90		ns
LVCMOS33_S16	1.79	1.91	2.10		3.33	3.72	4.30		3.33	3.72	4.30		ns
LVCMOS33_F4	1.79	1.91	2.10		5.07	5.38	5.85		5.07	5.38	5.85		ns
LVCMOS33_F8	1.79	1.91	2.10		4.31	4.61	5.06		4.31	4.61	5.06		ns
LVCMOS33_F12	1.79	1.91	2.10		2.74	3.45	4.52		2.74	3.45	4.52		ns
LVCMOS33_F16	1.79	1.91	2.10		2.62	2.88	3.29		2.62	2.88	3.29		ns
LVCMOS25_S4	1.50	1.60	1.74		4.98	5.47	6.21		4.98	5.47	6.21		ns
LVCMOS25_S8	1.50	1.60	1.74		3.91	4.35	5.01		3.91	4.35	5.01		ns
LVCMOS25_S12	1.50	1.60	1.74		3.10	3.65	4.49		3.10	3.65	4.49		ns
LVCMOS25_S16	1.50	1.60	1.74		3.55	3.99	4.65		3.55	3.99	4.65		ns
LVCMOS25_F4	1.50	1.60	1.74		4.72	5.08	5.63		4.72	5.08	5.63		ns
LVCMOS25_F8	1.50	1.60	1.74		2.75	3.31	4.14		2.75	3.31	4.14		ns
LVCMOS25_F12	1.50	1.60	1.74		2.75	3.30	4.14		2.75	3.30	4.14		ns
LVCMOS25_F16	1.50	1.60	1.74		2.20	2.54	3.06		2.20	2.54	3.06		ns
LVCMOS18_S4	0.79	0.84	0.90		3.74	3.96	4.28		3.74	3.96	4.28		ns
LVCMOS18_S8	0.79	0.84	0.90		2.94	3.29	3.83		2.94	3.29	3.83		ns
LVCMOS18_S12	0.79	0.84	0.90		2.94	3.29	3.83		2.94	3.29	3.83		ns
LVCMOS18_S16	0.79	0.84	0.90		2.03	2.28	2.66		2.03	2.28	2.66		ns
LVCMOS18_S24	0.79	0.84	0.90		1.89	2.09	2.37		1.89	2.09	2.37		ns
LVCMOS18_F4	0.79	0.84	0.90		3.60	3.77	4.02		3.60	3.77	4.02		ns
LVCMOS18_F8	0.79	0.84	0.90		2.14	2.48	2.98		2.14	2.48	2.98		ns
LVCMOS18_F12	0.79	0.84	0.90		2.14	2.48	2.98		2.14	2.48	2.98		ns
LVCMOS18_F16	0.79	0.84	0.90		1.62	1.79	2.05		1.62	1.79	2.05		ns
LVCMOS18_F24	0.79	0.84	0.90		1.37	1.50	1.69		1.37	1.50	1.69		ns
LVCMOS15_S4	0.81	0.87	0.96		4.17	4.42	4.80		4.17	4.42	4.80		ns
LVCMOS15_S8	0.81	0.87	0.96		2.53	2.87	3.38		2.53	2.87	3.38		ns

Table 27: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVCMOS15_S12	0.81	0.87	0.96		2.03	2.25	2.60		2.03	2.25	2.60		ns
LVCMOS15_S16	0.81	0.87	0.96		1.93	2.13	2.45		1.93	2.13	2.45		ns
LVCMOS15_F4	0.81	0.87	0.96		3.98	4.21	4.55		3.98	4.21	4.55		ns
LVCMOS15_F8	0.81	0.87	0.96		1.87	2.12	2.50		1.87	2.12	2.50		ns
LVCMOS15_F12	0.81	0.87	0.96		1.45	1.60	1.82		1.45	1.60	1.82		ns
LVCMOS15_F16	0.81	0.87	0.96		1.42	1.56	1.77		1.42	1.56	1.77		ns
LVCMOS12_S4	0.91	0.97	1.05		4.69	5.09	5.69		4.69	5.09	5.69		ns
LVCMOS12_S8	0.91	0.97	1.05		3.19	3.68	4.41		3.19	3.68	4.41		ns
LVCMOS12_S12	0.91	0.97	1.05		2.34	2.66	3.14		2.34	2.66	3.14		ns
LVCMOS12_F4	0.91	0.97	1.05		4.14	4.44	4.89		4.14	4.44	4.89		ns
LVCMOS12_F8	0.91	0.97	1.05		1.99	2.62	3.57		1.99	2.62	3.57		ns
LVCMOS12_F12	0.91	0.97	1.05		1.65	1.85	2.15		1.65	1.85	2.15		ns
SSTL135_S	0.67	0.70	0.75		1.13	1.21	1.34		1.13	1.21	1.34		ns
SSTL15_S	0.67	0.72	0.79		1.13	1.21	1.34		1.13	1.21	1.34		ns
SSTL18_I_S	0.68	0.72	0.79		1.58	1.71	1.91		1.58	1.71	1.91		ns
SSTL18_II_S	0.68	0.72	0.79		1.12	1.21	1.33		1.12	1.21	1.33		ns
DIFF_SSTL135_S	0.65	0.72	0.82		1.13	1.21	1.34		1.13	1.21	1.34		ns
DIFF_SSTL15_S	0.72	0.76	0.83		1.13	1.21	1.34		1.13	1.21	1.34		ns
DIFF_SSTL18_I_S	0.73	0.78	0.86		1.53	1.66	1.85		1.53	1.66	1.85		ns
DIFF_SSTL18_II_S	0.73	0.78	0.86		1.09	1.17	1.28		1.09	1.17	1.28		ns
SSTL135_F	0.67	0.70	0.75		1.01	1.09	1.22		1.01	1.09	1.22		ns
SSTL15_F	0.67	0.72	0.79		1.00	1.08	1.21		1.00	1.08	1.21		ns
SSTL18_I_F	0.68	0.72	0.79		1.10	1.19	1.32		1.10	1.19	1.32		ns
SSTL18_II_F	0.68	0.72	0.79		0.99	1.07	1.19		0.99	1.07	1.19		ns
DIFF_SSTL135_F	0.65	0.72	0.82		1.01	1.09	1.22		1.01	1.09	1.22		ns
DIFF_SSTL15_F	0.72	0.76	0.83		1.00	1.08	1.21		1.00	1.08	1.21		ns
DIFF_SSTL18_I_F	0.73	0.78	0.86		1.06	1.14	1.27		1.06	1.14	1.27		ns
DIFF_SSTL18_II_F	0.73	0.78	0.86		0.96	1.04	1.16		0.96	1.04	1.16		ns

Table 28: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{IOTPHZ}	T input to Pad high-impedance	2.39	2.56	2.80		ns

Input/Output Logic Switching Characteristics

Table 29: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.36/ 0.07	0.42/ 0.08	0.51/ 0.10		ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	1.17/ –0.14	1.36/ –0.14	1.64/ –0.14		ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.13/ 0.31	0.15/ 0.35	0.18/ 0.40		ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IDELAY)	0.17/ 0.31	0.19/ 0.35	0.24/ 0.40		ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.22	0.24	0.28		ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.25	0.29	0.33		ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.57	0.63	0.73		ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.60	0.67	0.78		ns
T_{ICKQ}	CLK to Q outputs	0.64	0.71	0.82		ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	1.32	1.52	1.81		ns
T_{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	9.05	9.05	12.52		ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.74	0.78	0.84		ns, Min

Table 30: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.65/ –0.22	0.72/ –0.22	0.83/ –0.22		ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.15/ –0.06	0.18/ –0.06	0.22/ –0.06		ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.63/ –0.20	0.75/ –0.20	0.94/ –0.20		ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.62/ –0.21	0.70/ –0.21	0.82/ –0.21		ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.14/ –0.05	0.16/ –0.05	0.20/ –0.05		ns
Combinatorial						
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.92	1.04	1.22		ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out	0.37	0.42	0.49		ns
T_{RQ_OLOGIC}	SR pin to OQ/TQ out	0.66	0.76	0.90		ns
T_{GSRQ_OLOGIC}	Global Set/Reset to Q outputs	9.05	9.05	12.52		ns
Set/Reset						
T_{RPW_OLOGIC}	Minimum Pulse Width, SR inputs	0.74	0.78	0.84		ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 31: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.15/ 0.13	0.17/ 0.15	0.21/ 0.17		ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.26/ –0.03	0.30/ –0.03	0.37/ –0.03		ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.07/ 0.16	0.08/ 0.18	0.09/ 0.21		ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.03/ 0.14	0.03/ 0.16	0.04/ 0.20		ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IDELAY)(1)	0.06/ 0.11	0.07/ 0.12	0.09/ 0.14		ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	0.03/ 0.14	0.03/ 0.16	0.04/ 0.20		ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY)(1)	0.11/ 0.11	0.12/ 0.12	0.14/ 0.14		ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.70	0.78	0.90		ns
Propagation Delays						
T_{ISDO_DO}	D input to DO output pin	0.22	0.24	0.28		ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 32: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.56/ –0.21	0.64/ –0.21	0.74/ –0.21		ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.62/ –0.22	0.70/ –0.22	0.82/ –0.22		ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.56/ –0.22	0.66/ –0.22	0.80/ –0.22		ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.15/ –0.06	0.18/ –0.06	0.22/ –0.06		ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.85	0.97	1.15		ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.14/ –0.05	0.16/ –0.05	0.20/ –0.05		ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.33	0.37	0.44		ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.33	0.37	0.44		ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ Out	0.92	1.03	1.21		ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 33: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IDELAYCTRL						
T_{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.83	3.83	3.83		µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.0(1)	200	200	200		MHz
	Attribute REFCLK frequency = 300.0(1)	300	300	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10		MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	61.95	61.95	61.95		ns
IDELAY						
$T_{IDELAYRESOLUTION}$	IDELAY chain delay resolution	1/(32 x 2 x F_{REF})				ps
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0		ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	±6	±6	±6		ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	±11	±11	±11		ps per tap
$T_{IDELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY	560	560	495		MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin Setup/Hold with respect to C	–0.02/ 0.24	–0.02/ 0.29	–0.02/ 0.35		ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin Setup/Hold with respect to C	0.11/ 0.29	0.13/ 0.33	0.14/ 0.40		ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin Setup/Hold with respect to C	0.12/ 0.31	0.14/ 0.36	0.16/ 0.45		ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5		ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 34: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T_{ILO}	An – Dn LUT address to A	0.10	0.11	0.13		ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.27	0.30	0.36		ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.42	0.46	0.55		ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.94	1.05	1.27		ns, Max
T_{AXA}	AX inputs to AMUX output	0.62	0.69	0.84		ns, Max
T_{AXB}	AX inputs to BMUX output	0.58	0.66	0.83		ns, Max
T_{AXC}	AX inputs to CMUX output	0.60	0.68	0.82		ns, Max
T_{AXD}	AX inputs to DMUX output	0.68	0.75	0.90		ns, Max
T_{BXB}	BX inputs to BMUX output	0.51	0.57	0.69		ns, Max
T_{BXD}	BX inputs to DMUX output	0.62	0.69	0.82		ns, Max
T_{CXC}	CX inputs to CMUX output	0.42	0.48	0.58		ns, Max
T_{CXD}	CX inputs to DMUX output	0.53	0.59	0.71		ns, Max
T_{DXD}	DX inputs to DMUX output	0.52	0.58	0.70		ns, Max
T_{OPCYA}	An input to COUT output	0.53	0.60	0.73		ns, Max
T_{OPCYB}	Bn input to COUT output	0.51	0.57	0.70		ns, Max
T_{OPCYC}	Cn input to COUT output	0.42	0.48	0.59		ns, Max
T_{OPCYD}	Dn input to COUT output	0.42	0.48	0.59		ns, Max
T_{AXCY}	AX input to COUT output	0.45	0.50	0.60		ns, Max
T_{BXCY}	BX input to COUT output	0.39	0.43	0.52		ns, Max
T_{CXCY}	CX input to COUT output	0.30	0.34	0.41		ns, Max
T_{DXCY}	DX input to COUT output	0.30	0.33	0.40		ns, Max
T_{BYP}	CIN input to COUT output	0.10	0.10	0.12		ns, Max
T_{CINA}	CIN input to AMUX output	0.41	0.45	0.55		ns, Max
T_{CINB}	CIN input to BMUX output	0.37	0.43	0.53		ns, Max
T_{CINC}	CIN input to CMUX output	0.33	0.37	0.44		ns, Max
T_{CIND}	CIN input to DMUX output	0.38	0.43	0.52		ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.40	0.44	0.53		ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.53	0.66		ns, Max

Table 34: **CLB Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D Flip Flops	0.09/ 0.14	0.11/ 0.16	0.14 0.20		ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D Flip Flops	0.06/ 0.19	0.07/ 0.21	0.09/ 0.26		ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D Flip Flops	0.59/ 0.08	0.66/ 0.09	0.81/ 0.11		ns, Min
T_{CECK_CLB}/ T_{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.15/ 0.00	0.17/ 0.00	0.21/ 0.01		ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.38/ 0.03	0.43/ 0.04	0.53/ 0.05		ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.28/ 0.17	0.31/ 0.19	0.38/ 0.23		ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.59	0.89	1.18		ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.53	0.59	0.71		ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.58	0.70		ns, Max
F_{TOG}	Toggle frequency (for export control)	1412	1286	1098		MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.
2. These items are of interest for Carry Chain applications.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 35: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T_{SHCKO}	Clock to A – B outputs	0.98	1.09	1.32		ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.37	1.53	1.86		ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK	0.54/ 0.28	0.60/ 0.30	0.72/ 0.35		ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock	0.27/ 0.55	0.30/ 0.60	0.37/ 0.70		ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.69/ 0.18	0.77/ 0.21	0.94/ 0.26		ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock	0.38/ 0.10	0.43/ 0.10	0.53/ 0.12		ns, Min
T_{CECK_LRAM}/ T_{CKCE_LRAM}	CE input to CLK	0.39/ 0.10	0.44/ 0.10	0.53/ 0.11		ns, Min
Clock CLK						
T_{MPW_LRAM}	Minimum pulse width	0.70	0.82	1.00		ns, Min
T_{MCP}	Minimum clock period	1.40	1.64	2.00		ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 36: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.19	1.21	1.30		ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.58	1.65	1.83		ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.09	1.14	1.27		ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS_SHFREG}/ T_{WH_SHFREG}	WE input	0.37/ 0.10	0.37/ 0.11	0.37/ 0.13		ns, Min
T_{CECK_SHFREG}/ T_{CKCE_SHFREG}	CE input to CLK	0.37/ 0.10	0.37/ 0.11	0.37/ 0.13		ns, Min
T_{DS_SHFREG}/ T_{DH_SHFREG}	A – D inputs to CLK	0.33/ 0.34	0.35/ 0.35	0.40/ 0.39		ns, Min
Clock CLK						
T_{MPW_SHFREG}	Minimum pulse width	0.60	0.70	0.85		ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.

Block RAM and FIFO Switching Characteristics

Table 37: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	2.10	2.33	2.68		ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.64	0.71	0.83		ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.77	3.20	3.84		ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.73	0.81	0.94		ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	2.61	2.88	3.30		ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	1.16	1.28	1.46		ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.76	0.83	0.92		ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.94	1.02	1.15		ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.78	0.85	0.94		ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register)	2.56	2.95	3.55		ns, Max
	Clock CLK to BITERR (with output register)	0.68	0.76	0.89		ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.75	0.83	0.94		ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.84	0.93	1.08		ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDRA}/T_{RCKC\_ADDRA}$	ADDR inputs[8]	0.45/ 0.26	0.49/ 0.28	0.57/ 0.31		ns, Min
$T_{RDCK\_DI\_WF\_NC}/$ $T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9]	0.58/ 0.26	0.65/ 0.28	0.74/ 0.30		ns, Min
$T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode[9]	0.20/ 0.26	0.22/ 0.28	0.25/ 0.30		ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.50/ 0.29	0.55 0.31	0.63/ 0.33		ns, Min
	DIN inputs with block RAM ECC encode only[9]	0.93/ 0.29	1.02/ 0.31	1.17/ 0.33		ns, Min
	DIN inputs with FIFO ECC in standard mode[9]	1.04/ 0.29	1.15/ 0.31	1.32/ 0.33		ns, Min
$T_{RCCK\_CLK}/T_{RCKC\_CLK}$	Inject single/double bit error in ECC mode	0.58/ 0.24	0.64/ 0.25	0.74/ 0.26		ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	Block RAM Enable (EN) input	0.35/ 0.20	0.39/ 0.21	0.45/ 0.23		ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.24/ 0.07	0.29/ 0.07	0.36/ 0.08		ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input[10]	0.29/ 0.04	0.32/ 0.04	0.35/ 0.05		ns, Min

Table 37: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.32/ 0.16	0.33/ 0.18	0.36/ 0.19		ns, Min
$T_{RCCK\_WEA}/T_{RCKC\_WEA}$	Write Enable (WE) input (Block RAM only)	0.44/ 0.18	0.48/ 0.19	0.54/ 0.20		ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.52/ 0.20	0.57/ 0.21	0.66/ 0.23		ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.49/ 0.20	0.54/ 0.21	0.62/ 0.23		ns, Min
Reset Delays (Flags)						
T_{RCO_RST}	Reset RST to FIFO Flags/Pointers(11)	0.90	0.98	1.10		ns, Max
Maximum Frequency						
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (Write first and No change modes) When not in SDP RF mode	509	461	388		MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	509	461	388		MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	447	404	339		MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	467	418	345		MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	467	418	345		MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	405	362	297		MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	509	461	388		MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	410	365	297		MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).
11. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.

DSP48E1 Switching Characteristics

Table 38: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.26/ 0.12	0.30/ 0.13	0.37/ 0.14		ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.33/ 0.15	0.38/ 0.16	0.45/ 0.18		ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.17/ 0.17	0.20/ 0.19	0.24/ 0.21		ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.25/ 0.18	0.32/ 0.20	0.42/ 0.22		ns
$T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.23/ 0.12	0.27/ 0.13	0.32/ 0.14		ns
$T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.25/ 0.15	0.29/ 0.16	0.36/ 0.18		ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$	{A, B} input to M register CLK using multiplier	2.40/ –0.01	2.76/ –0.01	3.29/ –0.01		ns
$T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$	{A, D} input to AD register CLK	1.29/ –0.02	1.48/ –0.02	1.76/ –0.02		ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\} \_PREG\_MULT}$	{A, B} input to P register CLK using multiplier	4.02/ –0.28	4.60/ –0.28	5.48/ –0.28		ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.93/ –0.73	4.50/ –0.73	5.35/ –0.73		ns
$T_{DSPDCK\_\{A, B\} \_PREG}$/ $T_{DSPCKD\_\{A, B\} \_PREG}$	A or B input to P register CLK not using multiplier	1.73/ –0.28	1.98/ –0.28	2.35/ –0.28		ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.54/ –0.26	1.76/ –0.26	2.10/ –0.26		ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.32/ –0.15	1.51/ –0.15	1.80/ –0.15		ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.35/ 0.06	0.42/ 0.08	0.52/ 0.11		ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.28/ 0.10	0.34/ 0.11	0.42/ 0.13		ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.36/ –0.03	0.43/ –0.03	0.52/ –0.03		ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.17/ 0.18	0.21/ 0.20	0.27/ 0.23		ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.36/ 0.01	0.43/ 0.01	0.53/ 0.01		ns

Table 38: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA;\ RSTB\}\_\{AREG;\ BREG\}}$/ $T_{DSPCKD\_\{RSTA;\ RSTB\}\_\{AREG;\ BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/ 0.11	0.46/ 0.13	0.55/ 0.15		ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/ 0.10	0.08/ 0.11	0.09/ 0.12		ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/ 0.07	0.50/ 0.08	059/ 0.09		ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/ 0.22	0.23/ 0.24	0.27/ 0.28		ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.27/ 0.01	0.30/ 0.01	0.35/ 0.01		ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.79	4.35	5.18		ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.72	4.26	5.07		ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier	1.53	1.75	2.08		ns
$T_{DSPDO\_C\_P}$	C input to P output	1.33	1.53	1.82		ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{DSPDO\_\{A;\ B\}\_\{ACOUT;\ BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.55	0.63	0.74		ns
$T_{DSPDO\_\{A,\ B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	4.06	4.65	5.54		ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.97	4.54	5.40		ns
$T_{DSPDO\_\{A,\ B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.77	2.03	2.41		ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.58	1.81	2.15		ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.65	4.19	5.00		ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.37	1.57	1.88		ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.38	0.44	0.53		ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.90	4.47	5.33		ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.61	1.85	2.21		ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	1.11	1.28	1.52		ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.36	1.56	1.85		ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output	0.33	0.37	0.44		ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output	0.52	0.59	0.69		ns

Table 38: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output	1.68	1.93	2.31		ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output	1.92	2.21	2.64		ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier	2.72	3.10	3.69		ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.96	3.38	4.02		ns
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.94	4.51	5.37		ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.64	1.87	2.22		ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.69	1.93	2.30		ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.91	4.48	5.32		ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87		ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70		ns
$T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55		ns
$T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65		ns
$T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63		ns
Maximum Frequency						
F_{MAX}	With all registers used	628	550	464		MHz
F_{MAX_PATDET}	With pattern detector	531	465	392		MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	349	305	257		MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	317	277	233		MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	397	346	290		MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	397	346	290		MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260	227	190		MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	241	211	177		MHz

Configuration Switching Characteristics

Table 39: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T_{PL}(1)	Program latency	5	5	5		ms, Max
T_{POR}(1)	Power-on reset	50	50	50		ms, Max
$T_{PROGRAM}$	Program pulse width	250	250	250		ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay	150	150	150		ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60		%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60		%, Min/Max
F_{MCCK}	Master CCLK frequency	100	100	100		MHz, Max
	Master CCLK frequency for AES encrypted x16	50	50	50		MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration	3	3	3		MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50		%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5		ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5		ns, Min
F_{SCCK}	Slave CCLK frequency	100	100	100		MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time	2.5	2.5	2.5		ns, Min
T_{EMCCKH}	External master CCLK High time	2.5	2.5	2.5		ns, Min
F_{EMCCK}	External master CCLK frequency	100	100	100		MHz, Max
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN Setup/Hold	5.0/0.0	5.0/0.0	5.0/0.0		ns, Min
T_{CCO}	DOUT clock to out	8.5	8.5	8.5		ns, Max
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	D[31:00] Setup/Hold	5.0/0.0	5.0/0.0	5.0/0.0		ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	5.0/0.0	5.0/0.0	5.0/0.0		ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	10.0/0.0		ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	8.5	8.5	8.5		ns, Max
T_{SMCO}	D[31:00] clock to out in readback	8.5	8.5	8.5		ns, Max
F_{RBCCK}	Readback frequency	100	100	100		MHz, Max

Table 39: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup/Hold	3.0/2.0	3.0/2.0	3.0/2.0		ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	8.5	8.5	8.5		ns, Max
F_{TCK}	TCK frequency	66	66	66		MHz, Max
BPI Master Flash Mode Programming Switching						
T_{BPICCO}(2)	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.5	8.5	8.5		ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] Setup/Hold	5.0/0.0	5.0/0.0	5.0/0.0		ns, Min
SPI Master Flash Mode Programming Switching						
T_{SPIDCC}/T_{SPICCD}	D[03:00] Setup/Hold	5.0/0.0	5.0/0.0	5.0/0.0		ns, Min
T_{SPICCM}	MOSI clock to out	8.5	8.5	8.5		ns, Max
$T_{SPICCFC}$	FCS_B clock to out	8.5	8.5	8.5		ns, Max
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
$T_{MMCMDCK\_DADDR}/T_{MMCMCKD\_DADDR}$	DADDR Setup/Hold	1.30/0.00	1.46/0.00	1.69/0.00		ns, Min
$T_{MMCMDCK\_DI}/T_{MMCMCKD\_DI}$	DI Setup/Hold	1.30/0.00	1.46/0.00	1.69/0.00		ns, Min
$T_{MMCMDCK\_DEN}/T_{MMCMCKD\_DEN}$	DEN Setup/Hold	1.83/0.00	2.05/0.00	2.39/0.00		ns, Min
$T_{MMCMDCK\_DWE}/T_{MMCMCKD\_DWE}$	DWE Setup/Hold	1.30/0.00	1.46/0.00	1.69/0.00		ns, Min
$T_{MMCMCKO\_DO}$	CLK to out of DO(3)	3.13	3.65	4.42		ns, Max
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.44	0.50	0.59		ns, Max
F_{DCK}	DCLK frequency	200	200	200		MHz, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in UG470: *7 Series FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 40: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	0.13/ 0.05	0.16/ 0.05	0.21/ 0.06		ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	0.13/ 0.05	0.16/ 0.05	0.21/ 0.06		ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.10	0.11	0.14		ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	628	550	464		MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 41: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BIOCKO_O}	Clock to out delay from I to O	1.35	1.52	1.79		ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	680	680	600		MHz

Table 42: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BRCKO_O}	Clock to out delay from I to O	0.91	1.03	1.21		ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.46	0.52	0.62		ns
T_{BRDO_O}	Propagation delay from CLR to O	0.79	0.90	1.05		ns
Maximum Frequency						
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	420	375	315		MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 43: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.3		ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	0.13/ 0.05	0.16/ 0.06	0.21/ 0.06		ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	628	550	464		MHz

MMCM Switching Characteristics

Table 44: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$MMCM\_F_{INMAX}$	Maximum Input Clock Frequency	800	800	800		MHz
$MMCM\_F_{INMIN}$	Minimum Input Clock Frequency	10	10	10		MHz
$MMCM\_F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
$MMCM\_F_{INDUTY}$	Allowable Input Duty Cycle: 10—49 MHz	25	25	25		%
	Allowable Input Duty Cycle: 50—199 MHz	30	30	30		%
	Allowable Input Duty Cycle: 200—399 MHz	35	35	35		%
	Allowable Input Duty Cycle: 400—499 MHz	40	40	40		%
	Allowable Input Duty Cycle: >500 MHz	45	45	45		%
$MMCM\_F_{MIN\_PSCLK}$	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01		MHz
$MMCM\_F_{MAX\_PSCLK}$	Maximum Dynamic Phase Shift Clock Frequency	550	500	450		MHz
$MMCM\_F_{VCOMIN}$	Minimum MMCM VCO Frequency	600	600	600		MHz
$MMCM\_F_{VCOMAX}$	Maximum MMCM VCO Frequency	1600	1440	1200		MHz
$MMCM\_F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical(1)	1.00	1.00	1.00		MHz
	High MMCM Bandwidth at Typical(1)	4.00	4.00	4.00		MHz
$MMCM\_T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs(2)	0.12	0.12	0.12		ns
$MMCM\_T_{OUTJITTER}$	MMCM Output Jitter(3)	Note 1				
$MMCM\_T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision(4)	0.16	0.21	0.21		ns
$MMCM\_T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	100		µs
$MMCM\_F_{OUTMAX}$	MMCM Maximum Output Frequency	800	800	800		MHz
$MMCM\_F_{OUTMIN}$	MMCM Minimum Output Frequency(5)(6)	4.69	4.69	4.69		MHz
$MMCM\_T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
$MMCM\_RST_{MINPULSE}$	Minimum Reset Pulse Width	5.00	5.00	5.00		ns
$MMCM\_F_{PFDMAX}$	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550	500	450		MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300		MHz
$MMCM\_F_{PFDMIN}$	Minimum Frequency at the Phase Frequency Detector	10	10	10		MHz
$MMCM\_T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				

Table 44: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM Switching Characteristics Setup and Hold						
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and Hold of Phase Shift Enable	1.09/ 0.00	1.09/ 0.00	1.09/ 0.00		ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.09/ 0.00	1.09/ 0.00	1.09/ 0.00		ns
$T_{MMCMCKO\_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.59	0.68	0.81		ns

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 45: **PLL Specification**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F_{INMAX}	Maximum Input Clock Frequency	800	800	800		MHz
PLL_F_{INMIN}	Minimum Input Clock Frequency	19	19	19		MHz
PLL_$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Allowable Input Duty Cycle: 19—49 MHz	25	25	25		%
	Allowable Input Duty Cycle: 50—199 MHz	30	30	30		%
	Allowable Input Duty Cycle: 200—399 MHz	35	35	35		%
	Allowable Input Duty Cycle: 400—499 MHz	40	40	40		%
	Allowable Input Duty Cycle: >500 MHz	45	45	45		%
PLL_F_{VCOMIN}	Minimum PLL VCO Frequency	800	800	800		MHz
PLL_F_{VCOMAX}	Maximum PLL VCO Frequency	2133	1866	1600		MHz
PLL_$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical(1)	1.00	1.00	1.00		MHz
	High PLL Bandwidth at Typical(1)	4.00	4.00	4.00		MHz
PLL_$T_{STATPHAOFFSET}$	Static Phase Offset of the PLL Outputs(2)	0.12	0.12	0.12		ns
PLL_$T_{OUTJITTER}$	PLL Output Jitter(3)	Note 1				
PLL_$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision(4)	0.15	0.20	0.20		ns
PLL_$T_{LOCKMAX}$	PLL Maximum Lock Time	100	100	100		µs
PLL_F_{OUTMAX}	PLL Maximum Output Frequency	800	800	800		MHz
PLL_F_{OUTMIN}	PLL Minimum Output Frequency(5)	6.25	6.25	6.25		MHz
PLL_$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
PLL_$RST_{MINPULSE}$	Minimum Reset Pulse Width	5.00	5.00	5.00		ns

Table 45: **PLL Specification *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550	500	450		MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300		MHz
PLL_F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	19	19	19		MHz
PLL_$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
PLL Switching Characteristics Setup and Hold						
T_{PLLCCK_DEN}/ T_{PLLCKC_DEN}	Setup and Hold of D enable	1.76/ 0.00	1.97/ 0.00	2.29/ 0.00		ns
T_{PLLCCK_DADDR}/ T_{PLLCKC_DADDR}	Setup and Hold of D address	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00		ns
T_{PLLCCK_DI}/ T_{PLLCKC_DI}	Setup and Hold of D input	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00		ns
T_{PLLCCK_DWE}/ T_{PLLCKC_DWE}	Setup and Hold of D write enable	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00		ns

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Artix-7 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 46: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF}	Clock-capable clock input and OUTFF *without* MMCM/PLL (near clock region)	XC7A8	6.38	7.22	8.53		ns
		XC7A15	6.38	7.22	8.53		ns
		XC7A30T	6.58	7.45	8.78		ns
		XC7A50T	6.58	7.45	8.78		ns
		XC7A100T	6.61	7.48	8.82		ns
		XC7A200T	7.10	7.98	9.32		ns
		XC7A350T	7.31	8.22	9.64		ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 47: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.							
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF *without* MMCM/PLL (far clock region)	XC7A8	6.38	7.22	8.53		ns
		XC7A15	6.38	7.22	8.53		ns
		XC7A30T	6.59	7.45	8.78		ns
		XC7A50T	6.59	7.45	8.78		ns
		XC7A100T	6.96	7.86	9.26		ns
		XC7A200T	7.82	8.77	10.22		ns
		XC7A350T	8.03	9.01	10.55		ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 48: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7A8	3.45	3.87	4.51		ns
		XC7A15	3.45	3.87	4.51		ns
		XC7A30T	3.48	3.91	4.55		ns
		XC7A50T	3.48	3.91	4.55		ns
		XC7A100T	3.72	4.18	4.86		ns
		XC7A200T	3.60	4.03	4.66		ns
		XC7A350T	3.68	4.14	4.87		ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 49: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.							
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7A8	3.34	3.77	4.41		ns
		XC7A15	3.34	3.77	4.41		ns
		XC7A30T	3.38	3.80	4.45		ns
		XC7A50T	3.38	3.80	4.45		ns
		XC7A100T	3.62	4.07	4.76		ns
		XC7A200T	3.49	3.93	4.56		ns
		XC7A350T	3.58	4.03	4.76		ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Artix-7 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 50: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks	XC7A8	1.35/ 0.73	1.44/ 0.87	1.55/ 1.12		ns
		XC7A15	1.35/ 0.73	1.44/ 0.87	1.55/ 1.12		ns
		XC7A30T	2.05/ 0.35	2.22/ 0.44	2.45/ 0.62		ns
		XC7A50T	2.05/ 0.35	2.22/ 0.44	2.45/ 0.62		ns
		XC7A100T	1.88/ 0.72	2.04/ 0.85	2.24/ 1.09		ns
		XC7A200T	2.22/ 0.81	2.43/ 0.91	2.72/ 1.08		ns
		XC7A350T	2.01/ 1.01	2.22/ 1.13	2.53/ 1.39		ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Table 51: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay clock-capable clock input and IFF(2) with MMCM	XC7A8	1.11/ 0.51	1.16/ 0.54	1.22/ 0.60		ns
		XC7A15	1.11/ 0.51	1.16/ 0.54	1.22/ 0.60		ns
		XC7A30T	1.23/ 0.54	1.29/ 0.58	1.36/ 0.64		ns
		XC7A50T	1.23/ 0.54	1.29/ 0.58	1.36/ 0.64		ns
		XC7A100T	1.39/ 0.78	1.47/ 0.85	1.58/ 0.95		ns
		XC7A200T	1.49/ 0.66	1.56/ 0.70	1.65/ 0.75		ns
		XC7A350T	1.36/ 0.74	1.43/ 0.81	1.53/ 0.95		ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 52: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No Delay clock-capable clock input and IFF(2) with PLL	XC7A8	1.02/ 0.40	1.06/ 0.44	1.12/ 0.50		ns
		XC7A15	1.02/ 0.40	1.06/ 0.44	1.12/ 0.50		ns
		XC7A30T	1.14/ 0.44	1.19/ 0.47	1.27/ 0.53		ns
		XC7A50T	1.14/ 0.44	1.19/ 0.47	1.27/ 0.53		ns
		XC7A100T	1.30/ 0.68	1.37/ 0.74	1.48/ 0.85		ns
		XC7A200T	1.39/ 0.55	1.46/ 0.60	1.55/ 0.64		ns
		XC7A350T	1.26/ 0.64	1.33/ 0.71	1.44/ 0.85		ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

Table 53: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	0.15	0.15	0.15		ns
T_{CKSKEW}	Global Clock Tree Skew(2)	XC7A8	0.04	0.04	0.04		ns
		XC7A15	0.04	0.04	0.04		ns
		XC7A30T	0.20	0.21	0.24		ns
		XC7A50T	0.20	0.21	0.24		ns
		XC7A100T	0.20	0.21	0.24		ns
		XC7A200T	0.39	0.42	0.47		ns
		XC7A350T	0.50	0.55	0.69		ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.10	0.10	0.10		ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.04	0.04	0.03		ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.18	0.18	0.18		ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 54: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC7A8	CPG236		ps
			CSG324		ps
			FTG256		ps
		XC7A15	CPG236		ps
			CSG324		ps
			FTG256		ps
		XC7A30T	CSG225		ps
			CSG324		ps
			FTG256		ps
			FGG484		ps
		XC7A50T	CSG225		ps
			CSG324		ps
			FTG256		ps
			FGG484		ps
		XC7A100T	CSG324		ps
			FTG256		ps
			FGG484		ps
			FGG676		ps
		XC7A200T	FBG484		ps
			FBG676		ps
			FFG1156		ps
		XC7A350T	FBG484		ps
			FBG676		ps
			FFG1156		ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 55: **Sample Window**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{SAMP}	Sampling Error at Receiver Pins(1)	0.61	0.67	0.72		ns
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	0.36	0.42	0.48		ns

Notes:

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 56: **Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO						
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.27/ 1.99	–0.27/ 2.21	–0.27/ 2.56		ns
Pin-to-Pin Clock-to-Out Using BUFIO						
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	6.84	7.75	9.15		ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description
09/26/11	1.0	Initial Xilinx release.
11/07/11	1.1	Revised the V_{OCM} specification in Table 8. Updated the Switching Characteristics based upon the ISE 13.3 software v1.02 speed specification throughout document including Table 25 and Table 26. Added MMCM_$T_{FBDELAY}$ while adding MMCM_ to the symbol names of a few specifications in Table 44 and PLL to the symbol names in Table 45. In Table 46 through Table 52, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 55.

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